REMARKS

Reconsideration of this application is respectfully requested in view of the foregoing amendment and the following remarks.

By the foregoing amendment, claims 1, 5-8, 17 and 18 have been deleted, and claims 10 and 12 have been amended. Claims 10-12 are now pending.

Amended claim 10 sets forth a mounting structure of a semiconductor device on a circuit substrate. The semiconductor device includes a protective package. The circuit substrate includes a first surface formed with a predetermined wiring pattern, and a second surface opposite to the first surface. The circuit board also includes a through hole corresponding to a shape of the protective package. The protective package of the semiconductor device is fitted into the through hole of the substrate while partially projecting beyond the first and second surfaces of the substrate.

The above-described features are best shown in Fig. 4 of the present application. As shown in that figure, the protective package 4' is shown to be fitted in the through hole 50a of the circuit substrate 5 while projecting above and below the substrate 5. Such a mounting structure is advantageous in that the thickness of the substrate 5 is not additional to the thickness or height of the protective package 4'.

As noted by the Examiner, US Patent No. 5,495,125 to Uemura fails to disclose a circuit substrate, let alone a through hole of such a substrate for receiving a resin package of a semiconductor device.

With regard to US Patent No. 5,198,888 to Sugano et al., it appears that the Examiner has improperly equated each of the connectors 9a-9d with the claimed circuit substrate of the present invention. Note that the element numbered 20 is a substrate that corresponds to the claimed circuit substrate of the present invention. Further, even if each connector 9a-9d is regarded as equivalent to the claimed circuit substrate of the present invention, the protective package is not considered to project above and below beyond the two opposite surfaces of the connector.

Like Uemura, JP 01-120875 even fails to disclose a circuit substrate, let alone a through hole of such a substrate for receiving a resin package of a semiconductor device.

In view of the foregoing all of the claims in this case are believed to be in condition for allowance. Should the Examiner have any questions or determine that any further action is desirable to place this application in even better condition for issue, the Examiner is encouraged to telephone applicants' undersigned representative at the number listed below.

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Respectfully submitted,

SHINICHI SUZUKI, ET AL.

Date: February 20, 2003

By: _____
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Attachments: Amended Claims w/ Markings

MDB/lrhj

Customer No. 28970

VERSION WITH MARKINGS TO SHOW CHANGES MADE TO CLAIMS

1. (Cancel)

5. (Cancel)

6 (Cancel)

7. (Cancel)

8. (Cancel)

10. (Amended) A mounting structure of a semiconductor device on a circuit substrate,

the semiconductor device including: a semiconductor chip; a protective package for covering the semiconductor chip, including at least a pair of opposed side surfaces, each of the side surfaces having a first slanted portion and a second slanted portion each being flat and meeting the other at a predetermined angle; a first lead conducting to the semiconductor chip, including an inner portion covered by the protective package and a plurality of outer portions extending out of the protective package; a second lead conducting to the semiconductor chip, including an inner portion covered by the protective package and a plurality of outer portions extending out of the protective package; the inner portions and the outer portions of the first and

the second leads being flat and extending in a same plane; the outer portions of the first lead extending from both of the pair of opposed side surfaces out of the protective package; the outer portions of the second lead extending from both of the opposed side surfaces out of the protective package;

the circuit substrate including: a [main] first surface formed with a predetermined wiring pattern; a second surface opposite to the first surface; a plurality of connecting pads formed in the [main] first surface; and a through hole corresponding to a shape of the protective package;

wherein the protective package is fitted into the through hole of the substrate while partially projecting beyond the first and second surfaces of the substrate, [and] the outer portions of the first lead and the second lead [are] being connected with the connecting pads.

12. (Amended) The mounting structure according to Claim 10, wherein the [main] first surface mounted with the semiconductor device is laminated with a coating member.

17. (Cancel)

18. (Cancel)